SEMESTER S7

LOW POWER VLSI DESIGN

Course Code	PEEVT741	CIE Marks	40
Teaching Hours/Week (L: T:P: R)	3:0:0:0	ESE Marks	60
Credits	3	Exam Hours	2 Hrs. 30 Min.
Prerequisites (if any)	None	Course Type	Theory

Course Objectives:

1. To impart knowledge on different sources of power dissipation, power minimization techniques, switched capacitance minimization and working principle of adiabatic logic circuits

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	**Physics of Power dissipation in MOSFET devices** Need for low power circuit design, MIS Structure **Deep submicron transistor design issues: Short channel effects** Channel Length Modulation , Surface scattering, Punch through, Velocity saturation, Impact ionization, Hot electron effects, Body Effect, Narrow width effect, V_{th} roll-off, Drain Induced Barrier Lowering, Gate Induced drain leakage, Tunneling Through Gate Oxide, Subthreshold Leakage Current, **Emerging Technologies for Low Power:** Hi-K Gate Dielectric, Lightly Doped Drain–Source, Silicon on Insulator,	9
2	**Sources of power dissipation in digital ICs** – **Dynamic Power Dissipation:** Short Circuit Power: Short Circuit Current of Inverter , Short circuit current dependency on input rise and fall time, Variation of shortcircuit current with load capacitance. Switching power dissipation: Switching Power of CMOS Inverter, Switching activity and its effects.	9

	Glitching Power: Glitches and its effect on power dissipation **Static Power Dissipation:** Sources of Leakage Power, Effects of V_{dd} and V_t on speed, Constraints on V_t Reduction.	
3	**Low-Power Design Approaches-** **Supply Voltage Scaling for Low Power:** Effect of Supply voltage on Delay and Power Effect of Supply voltage on Static and Dynamic Power Multi VDD ,Dynamic VDD, Dynamic Voltage and Frequency Scaling (DVFS) Approaches. Architectural Level Approaches: Pipelining and Parallel Processing **Leakage power reduction Techniques:** Effect of threshold voltage on Leakage Power Transistor stacking, MTCMOS, VTCMOS Power gating& Clock gating Techniques.	**9**
4	**Circuit Design Styles for Low Power-** **Non clocked circuit design style:** Fully Complementary logic. NMOS and Pseudo –NMOS logic, Differential Cascode Voltage Switch logic(DCVS) **Clocked design style:** Basic concept, Dynamic Logic, Domino logic, Differential Current Switch Logic. **Adiabatic switching** – Adiabatic charging, Adiabatic amplification, Adiabatic logic gates, Pulsed power supplies.	**9**

Course Assessment Method
(CIE: 40 marks, ESE: 60 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Assignment/ Microproject	Internal Examination-1 (Written)	Internal Examination- 2 (Written)	Total
5	**15**	**10**	**10**	**40**

End Semester Examination Marks (ESE)

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	Part B	Total
• 2 Questions from each module. • Total of 8 Questions, each carrying 3 marks **(8x3 =24marks)**	• Each question carries 9 marks. • Two questions will be given from each module, out of which 1 question should be answered. • Each question can have a maximum of 3 sub divisions. **(4x9 = 36 marks)**	**60**

Course Outcomes (COs)

At the end of the course students should be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	Describe the impact of technology scaling on power dissipation in digital ICs and various short channel effects	K2
CO2	Discuss the different sources of power dissipation in digital ICs.	K2
CO3	Describe the various approaches for power management in digital ICs.	K2
CO4	Apply various clocked and non-clocked design styles for logic implementation	K3
CO5	Describe the use of Adiabatic switching for power management in digital ICs.	K2

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO-PO Mapping Table (Mapping of Course Outcomes to Program Outcomes)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	**3**											**2**
CO2	**3**											**2**
CO3	**3**			**2**								**2**
CO4	**3**	**2**	**3**		**3**							**2**
CO5	**3**											**2**

Note: *1: Slight (Low), 2: Moderate (Medium), 3: Substantial (High), -: No Correlation*

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Design of Analog CMOS Integrated Circuits	Behzad Razavi	McGraw-Hill	2/e, 2002
2	CMOS: Circuits Design, Layout and Simulation,	Baker, Li, Boyce,	Prentice Hall India,	2000
3	Microelectronic Circuits	Sedra & Smith	Oxford University Press	6/e,2017

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	CMOS Analog Circuit Design,	Phillip E. Allen, Douglas R. Holbery	Oxford University Press	3/e
2	Fundamentals of Microelectronics	Behzad Razavi	Wiley student Edition	2014
3	Analysis and Design of Analog Integrated Circuits	Meyer Gray , Hurst, Lewis	Wiley	5/e, 2009

Video Links (NPTEL, SWAYAM…)	
Module No.	**Link ID**
1	www.youtube.com/@b_razavi, www.youtube.com/@analogicdesign-iitm5234
2	www.youtube.com/@b_razavi, www.youtube.com/@analogicdesign-iitm5234
3	www.youtube.com/@b_razavi, www.youtube.com/@analogicdesign-iitm5234
4	Switching Circuits and Logic Design by Prof. Indranil Sengupta Lectures 47-51