SEMESTER S5

FPGA BASED SYSTEM DESIGN

Course Code	PCEVT502	CIE Marks	40
Teaching Hours/Week (L: T:P: R)	3:1:0:0	ESE Marks	60
Credits	4	Exam Hours	2 Hrs. 30 Min.
Prerequisites (if any)	None	Course Type	Theory

Course Objectives:

1. This Course aims to inculcate the knowledge on advanced design and analysis of digital circuits with HDL. The primary goal is to provide in depth understanding of the system design. The course would enable the students to apply their knowledge for the design of advanced digital hardware systems with the help of FPGA tools.

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	**VERILOG HDL** :Verilog HDL Coding Style: Lexical Conventions - Ports and Modules – Operators - Gate Level Modeling - System Tasks & Compiler Directives - Test Bench - Data Flow Modeling - Behavioral level Modeling - Tasks & Functions	11
2	**FPGA ARCHITECTURE**: FPGA Architectural options, coarse vs fine grained, vendor specific issues (emphasis on Xilinx FPGA), Antifuse, SRAM and EPROM based FPGAs, FPGA logic cells, Interconnection network and I/O Pad	11
3	**VERILOG MODELLING** :Verilog Modelling of Combinational and Sequential Circuits: Behavioral, Data Flow and Structural Realization – Adders – Multipliers- Comparators - Flip Flops - Realization of Shift Register - Realization of a Counter- Synchronous and Asynchronous FIFO –Single port and Dual port RAM – Pseudo Random LFSR – Cyclic Redundancy Check	11
4	**XILLINX** :System Design Examples using Xillinx FPGAs – Traffic light Controller, Real Time Clock - Interfacing using FPGA: Keyboard, LCD **Commercial FPGAs:** Xilinx, Altera, Actel (Different series description only)	11

Course Assessment Method
(CIE: 40 marks, ESE: 60 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Assignment/ Microproject	Internal Examination-1 (Written)	Internal Examination- 2 (Written)	Total
5	15	10	10	40

End Semester Examination Marks (ESE)

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	Part B	Total
• 2 Questions from each module. • Total of 8 Questions, each carrying 3 marks **(8x3 =24marks)**	• Each question carries 9 marks. • Two questions will be given from each module, out of which 1 question should be answered. • Each question can have a maximum of 3 sub divisions. **(4x9 = 36 marks)**	**60**

Course Outcomes (COs)

At the end of the course students should be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	Understand complex combinational and sequential digital circuits.	**K2**
CO2	Apply Verilog HDL in modelling Combinational and sequential digital circuits	**K3**
CO3	Understand digital circuits with Verilog HDL at behavioural, structural, and RTL Levels	**K2**
CO4	Understand the FPGA Architecture and implement the combinational and sequential digital circuits in FPGA	**K2**

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO-PO Mapping Table (Mapping of Course Outcomes to Program Outcomes)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	**2**		**1**									**2**
CO2	**2**		**2**									**2**
CO3	**3**	**2**	**3**		**1**							**2**
CO4				**1**								**2**

Note: *1: Slight (Low), 2: Moderate (Medium), 3: Substantial (High), -: No Correlation*

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	FPGA Prototyping by Verilog Examples	Pong P. Chu	John Wiley & Sons	2008
2	Verilog HDL: A Guide to Digital Design and Synthesis	Samir Palnitkar	Prentice Hall PTR	Second Edition,2003

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Application Specific Integrated Circuits	M.J.S. Smith	Pearson	2000
2	Digital Design using VHDL	Peter Ashenden	Elsevier	2007
3	FPGA based system design	W. Wolf	Pearson	2004

Video Links (NPTEL, SWAYAM…)	
Module No.	**Link ID**
1	https://youtu.be/IXjNLK7GC70
2	https://youtu.be/vHLBO05TeyU?si=uef41ETWM7t95oiL