SEMESTER S4

DIGITAL SYSTEM DESIGN

Course Code	PCEVT402	CIE Marks	40
Teaching Hours/Week (L: T:P: R)	3:1:0:0	ESE Marks	60
Credits	4	Exam Hours	2 Hrs. 30 Min.
Prerequisites (if any)	PBECT304 Logic Circuit Design	Course Type	Theory

Course Objectives:

1. To equip students with comprehensive knowledge and skills in designing, analysing, modelling, and optimizing clocked synchronous sequential networks (CSSNs).
2. To provide a thorough understanding of the designing, analyzing, and optimizing techniques of asynchronous sequential circuits (ASCs).
3. To equip students with the knowledge and skills to identify and mitigate static and dynamic hazards and to understand fault detection and testing methods.
4. To provide students with a comprehensive understanding of the VLSI design flow and the application of VHDL constructs and coding for combinational and sequential circuits.

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	Clocked Synchronous Networks, Analysis of Clocked Synchronous Sequential Networks (CSSN), Modelling of CSSN, State assignment and reduction, Design of CSSN, ASM Chart and its realization.	11
2	Asynchronous Sequential Circuits, Analysis of Asynchronous Sequential Circuits (ASC), Flow table reduction, Races in ASC, State assignment problem and the transition table, Design of Asynchronous Sequential Circuits, Design of ALU.	11
3	Hazards – static and dynamic hazards in combinational networks, Essential Hazards, Design of Hazard free circuits, Data synchronizers, Mixed operating mode asynchronous circuits, Practical issues- clock skew and jitter, Synchronous and asynchronous inputs, Flip-Flops and	11

	Simple Flip-Flop Applications, switch debouncer. Faults, Fault table method – path sensitization method – Boolean difference method, Kohavi algorithm, Automatic test pattern generation – Built in Self-Test (BIST)	
4	VLSI Design flow: Design entry: Schematic, FSM & HDL, different modeling styles in VHDL, Data types and objects, Dataflow, Behavioral and Structural Modeling, Synthesis, simulation. VHDL constructs and codes for combinational and sequential circuits.	**11**

Course Assessment Method
(CIE: 40 mark , ESE: 60 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Assignment/ Microproject	Internal Examination-1 (Written)	Internal Examination-2 (Written)	Total
5	**15**	**10**	**10**	**40**

End Semester Examination Marks (ESE)

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	Part B	Total
• 2 Questions from each module. • Total of 8 Questions, each carrying 3 marks **(8x3 =24marks)**	• Each question carries 9 marks. • Two questions will be given from each module, out of which 1 question should be answered. • Each question can have a maximum of 3 sub divisions. **(4x9 = 36 marks)**	**60**

Course Outcomes (COs)

At the end of the course students should be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	Design, analyze, and model clocked synchronous sequential networks (CSSNs), optimize state assignment and reduction, and effectively utilize ASM charts for the realization of complex digital systems.	**K3**
CO2	Design and analyze asynchronous sequential circuits (ASCs), perform flow table reduction, address race conditions and state assignment problems, and design both ASCs and Arithmetic Logic Units (ALUs).	**K3**
CO3	Identify and mitigate static and dynamic hazards in combinational networks, design hazard-free circuits, address practical issues in digital systems and apply fault detection and testing methods.	**K2**
CO4	Understand the VLSI design flow, utilize various design entry methods, apply different VHDL modeling styles, and develop and simulate VHDL constructs for combinational and sequential circuits.	**K2**

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO-PO Mapping Table:

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	**3**	**2**	**2**									
CO2	**3**	**2**	**2**									
CO3	**3**	**1**	**2**									
CO4	**1**	**1**	**2**	**1**	**2**							
CO5												

1: Slight (Low), 2: Moderate (Medium), 3: Substantial (High), -: No Correlation

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Digital Principles & Design	Donald G Givone	McGraw Hill Education	2017
2	Digital Design: Principles and Practices	John F Wakerly	Pearson India	4th, 2008
3	Digital Logic Applications and Design	John M Yarbrough	Cengage Learning India	1st, 2006
4	Digital Design: With an Introduction to the Verilog HDL, VHDL, and SystemVerilog	M.Morris Mano and Michel.D.Ciletti,	Pearson	6th, 2017

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Digital Systems Testing and Testable Design	Melvin A. Breuer, Miron Abramovici, Arthur D. Friedman	Wiley-IEEE Press	1st, 1994
2	Logic Design Theory	Nripendra N. Biswas	Prentice Hall	1993
3	Introduction to Digital Design Using Digilent FPGA Boards: Block Diagram / VHDL Examples	Richard E. Haskell Darrin M. Hanna	LBE Books- LLC	2019
4	Digital Circuits and Logic Design	Samuel C. Lee	Prentice Hall India Learning Private Limited	1980
5	Switching and Finite Automata Theory	Zvi Kohavi, Niraj K. Jha	CAMBRIDGE UNIVERSITY PRESS	3rd 2009
6	Digital System Design Using VHDL	Rishabh Anand	Khanna Publishing	1st, 2013
7	Digital System Design Using VHDL	Lizy Kurian John, Charles H. Roth	Cengage	1st, 2012

Video Links (NPTEL, SWAYAM…)	
Module No.	**Link ID**
1	https://archive.nptel.ac.in/courses/117/106/117106086/
2	https://archive.nptel.ac.in/courses/117/106/117106086/
3	https://archive.nptel.ac.in/courses/108/105/108105132/ Lecture 15
4	https://nptel.ac.in/courses/108106177