SEMESTER S3

LOGIC CIRCUIT DESIGN LABORATORY

Course Code	**PCECL308**	**CIE Marks**	50
Teaching Hours/Week (L: T:P: R)	0:0:3:0	**ESE Marks**	50
Credits	2	**Exam Hours**	2 Hrs. 30 Min.
Prerequisites (if any)	None	**Course Type**	Lab

Course Objectives:

1. Familiarise the students with the Digital Logic Design through the implementation of Logic Circuits .
2. Familiarise the students with the HDL based Digital Design and FPGA boards.

Expt. No.	**Part A – List of Experiments using digital components (Any *Six* experiments mandatory)**
1	Realization of functions using basic and universal gates (SOP and POS forms).
2	Design and Realization of half/full adder and subtractor using basic gates and universal gates.
3	4 bit adder/subtractor and BCD adder using 7483
4	Study of Flip Flops : S-R, D, T, JK and Master slave JK FF using NAND gates
5	Asynchronous Counter : 3 bit up/down counter, Realization of Mod N Counter
6	Synchronous Counter: Realization of 4-bit up/down counter, Realization of Mod-N counters
7	Ring counter and Johnson Counter.
8	Realization of counters using IC's (7490, 7492, 7493).
9	Realization of combinational circuits using MUX & DEMUX, using ICs (74150, 74154)
10	Sequence Generator / Detector
Expt. No.	**Part B – Simulation Experiments (Any *Six* experiments mandatory)** The experiments shall be conducted using Verilog and implementation using small FPGA
1	Realization of Logic Gates and Familiarization of FPGAs (a) Familiarization of a small FPGA board and its ports and interface. (b) Create the .pcf files for your FPGA board. (c) Familiarization of the basic syntax of verilog

	(d) Development of verilog modules for basic gates, synthesis and implementation in the above FPGA to verify the truth tables. (e) Verify the universality and non associativity of NAND and NOR gates by uploading The corresponding verilog files to the FPGA boards.
2	Adders in Verilog (a) Development of verilog modules for half adder in any of the 3 modeling styles (b) Development of verilog modules for full adder in structural modeling using half adder.
3	Mux and Demux in Verilog (a) Development of verilog modules for a 4x1 MUX. (b) Development of verilog modules for a 1x4 DEMUX.
4	Flipflops and coutners (a) Development of verilog modules for SR, JK and D flipflops. (b) Development of verilog modules for a binary decade/Johnson/Ring counters
5	Multiplexer and Logic Implementation in FPGA (a) Make a gate level design of an 8 : 1 multiplexer, write to FPGA and test its functionality. (b) Use the above module to realize any logic function
6	Flip-Flops and their Conversion in FPGA (a) Make gate level designs of J-K, J-K master-slave, T and D flip-flops, implement and test them on the FPGA board. (b) Implement and test the conversions such as T to D, D to T, J-K to T and J-K to D
7	Asynchronous and Synchronous Counters in FPGA (a) Make a design of a 4-bit up down ripple counter using T-flip-flops in the previous experiment, implement and test them on the FPGA board. (b) Make a design of a 4-bit up down synchronous counter using T-flip-lops in the previous experiment, implement and test them on the FPGAboard.
8	Universal Shift Register in FPGA (a) Make a design of a 4-bit universal shift register using D-flip-flops in the previous experiment, implement and test them on the FPGA board. (b) Implement ring and Johnson counters with it.
9	BCD to Seven Segment Decoder in FPGA (a) Make a gate level design of a seven segment decoder, write to FPGA and test its functionality. (b) Test it with switches and seven segment display. Use ouput ports for connection to the display.

Course Assessment Method
(CIE: 50 marks, ESE: 50 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Preparation/Pre-Lab Work experiments, Viva and Timely completion of Lab Reports / Record (Continuous Assessment)	Internal Examination	Total
5	**25**	**20**	**50**

End Semester Examination Marks (ESE):

Procedure/ Preparatory work/Design/ Algorithm	Conduct of experiment/ Execution of work/ troubleshooting/ Programming	Result with valid inference/ Quality of Output	Viva voce	Record	Total
10	15	10	10	5	50

- ***Submission of Record: Students shall be allowed for the end semester examination only upon submitting the duly certified record.***
- ***Endorsement by External Examiner:*** *The external examiner shall endorse the record*

Course Outcomes (COs)

At the end of the course students should be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	Design and demonstrate the functioning of various combinational and sequential circuits using ICs	**K3**
CO2	Apply an industry compatible hardware description language to implement digital circuits	**K3**
CO3	Implement digital circuits on FPGA boards and connect external hardware to the boards	**K3**
CO4	Function effectively as an individual and in a team to accomplish the given task.	**K2**

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO- PO Mapping (Mapping of Course Outcomes with Program Outcomes)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	3	3	2					3			3
CO2	3	1	1	3	3				3	1		3
CO3	3	1	1	3	3				3	1		3
CO4	3	3	3		3				3			3

1: Slight (Low), 2: Moderate (Medium), 3: Substantial (High), -: No Correlation

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Verilog HDL Synthesis: A Practical Primer	. J. Bhasker	B. S. Publications, 2001	
2	Fundamentals of Logic Design	Roth C.H	Jaico Publishers. V Ed., 2009	5th Edition

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Verilog HDL :A guide to digital design and synthesis	Palnitkar S.,	Prentice Hall; 2003.	2nd Edn.,

Continuous Assessment (25 Marks)

1. Preparation and Pre-Lab Work (7 Marks)

- Pre-Lab Assignments: Assessment of pre-lab assignments or quizzes that test understanding of the upcoming experiment.
- Understanding of Theory: Evaluation based on students' preparation and understanding of the theoretical background related to the experiments.

2. Conduct of Experiments (7 Marks)

- Procedure and Execution: Adherence to correct procedures, accurate execution of experiments, and following safety protocols.
- Skill Proficiency: Proficiency in handling equipment, accuracy in observations, and troubleshooting skills during the experiments.
- Teamwork: Collaboration and participation in group experiments.

3. Lab Reports and Record Keeping (6 Marks)

- Quality of Reports: Clarity, completeness and accuracy of lab reports. Proper documentation of experiments, data analysis and conclusions.
- Timely Submission: Adhering to deadlines for submitting lab reports/rough record and maintaining a well-organized fair record.

4. **Viva Voce (5 Marks)**

- Oral Examination: Ability to explain the experiment, results and underlying principles during a viva voce session.

Final Marks Averaging: The final marks for preparation, conduct of experiments, viva, and record are the average of all the specified experiments in the syllabus.

Evaluation Pattern for End Semester Examination (50 Marks)

1. **Procedure/Preliminary Work/Design/Algorithm (10 Marks)**

- Procedure Understanding and Description: Clarity in explaining the procedure and understanding each step involved.
- Preliminary Work and Planning: Thoroughness in planning and organizing materials/equipment.
- Algorithm Development: Correctness and efficiency of the algorithm related to the experiment.
- Creativity and logic in algorithm or experimental design.

2. **Conduct of Experiment/Execution of Work/Programming (15 Marks)**

- Setup and Execution: Proper setup and accurate execution of the experiment or programming task.

3. **Result with Valid Inference/Quality of Output (10 Marks)**

- Accuracy of Results: Precision and correctness of the obtained results.
- Analysis and Interpretation: Validity of inferences drawn from the experiment or quality of program output.

4. **Viva Voce (10 Marks)**

- Ability to explain the experiment, procedure results and answer related questions
- Proficiency in answering questions related to theoretical and practical aspects of the subject.

5. **Record (5 Marks)**

- Completeness, clarity, and accuracy of the lab record submitted

SEMESTER 4

ELECTRONICS ENGINEERING (VLSI Design and Technology)